REMARKS

Claims 1-24 are currently pending in the present application. It is gratefully acknowledged that the Examiner still finds allowable subject matter in Claims 4-7, 9, 14-17, and 20.

In the Office Action the Examiner has rejected Claims 1, 8, 10, 11, 18, 19, and 21 under 35 U.S.C. § 102(b) as being anticipated by *Ariyoshi et al.* (U.S. 5,930,244), and Claims 2, 3, 12, 13, and 22-24 under 35 U.S.C. § 103(a) as being unpatentable over *Ariyoshi* in view of *Dean et al.* (U.S. 5,839,052). Additionally, the Examiner has objected to Claims 1, 10, 11, and 21.

With regard to the objections of Claims 1, 10, 11, and 21, applicants' representation contacted the Examiner to discuss his objection, or more so, explain the claims to the Examiner. No agreement was reached, but a better understanding of the claims was set forth.

Claims 10, 11, and 21, have been amended to correct inconsistent use of the terms "system time" and "system timing" in Claims 10 and 11, and the inconsistent use of the terms "starting time" and "starting timing" in Claim 21.

The Examiner has rejected independent Claims 1, 10, 11 and 21 under 35 U.S.C. § 102(b) as being anticipated by *Ariyoshi*. *Ariyoshi* does not teach the scrambling step as recited in these claims, i.e., scrambling a frame data with an orthogonal code and a scrambling code generated at a time being different from a generating time of the frame data *with a scrambling code offset calculated from the transmission time adjustment value.*

The claims of the present application relates to a method for synchronization of an uplink signal receiving time. A Node B provides a UE with a transmission time adjustment value and the UE uses a scrambling code offset calculated using the adjustment value. The Examiner asserted that this concept is corresponding to a PC-i and PS-i of *Ariyoshi*.

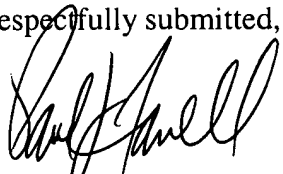
Ariyoshi is for synchronization of reverse links. See col. 2, lines 20-24, 36-38. In *Ariyoshi*, a reverse link phase synchronization control instruction PC-i of each terminal is determined in accordance with the contents of the phase of difference information PD-i. See col. 4, lines 35-42. *Ariyoshi* also describes a terminal outputting a control signal PS-i for fine adjustment of the phase of the orthogonal code Wi and pseudo noises PNr in accordance with PC-i.

However, *Ariyoshi* does **not** disclose that the PC-i corresponding to an adjustment value of the present invention is calculated using a time offset between a transmission time of the reference signal and a transmission time of a downlink DPCH. And, *Ariyoshi* does **not** disclose a scrambling code that is generated at a different time other than a start time of a frame data having a scrambling code offset calculated from a transmission time adjustment value.

Without conceding the patentability per se of dependent Claims 2, 3, 8, 12, 13, 18, 19 and 22-24, they are likewise believed to be allowable by virtue of their dependence on independent Claims 1, 11 and 21, respectively. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 2, 3, 8, 12, 13, 18, 19 and 22-24 are respectfully requested.

In view of the preceding amendments and remarks, it is respectfully submitted that all pending claims, namely Claims 1-24 are in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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